Spring 2012
CSE 320: Design and Synthesis of Digital Hardware
Monday/Wednesday: 2.00-3.15 pm
BYAC 240

Textbook
- No required textbook
- Optional: “The Designers Guide to VHDL” by P.R. Ashenden. [Excellent for VHDL]
- Optional: “HDL Chip Design” by Douglas J. Smith [Excellent for Synthesis]

Course Outcomes
- To provide computer systems engineering students with a fundamental understanding of hardware modeling with languages.
  o Students will understand modeling concurrency through event stepped simulation.
  o Students will be able partition designs for expediting design, reliability, resusability, and reconfigurability.
  o Students will be able to distinguish between executable models and executable implementations.
  o Students will understand the iteration and recursion constructs and their implication for synthesis.

- To gain the ability to develop synthesizable models using a hardware description language.
  o Students will write HDL programs for moderately sized digital systems requiring multi-level design and configuration control.
  o Students will analyze, verify and synthesize FPGA designs described in HDL.

- To gain the skill of designing and developing hardware prototypes using FPGA devices for hardware peripherals
  o Students understand the design and implementation process of FPGA devices, and are able to develop hardware prototypes
  o Students can develop efficient and synthesizable HDL code for FPGA devices.
  o Students understand the timing simulation and can use tools to verify timing

Major Topics Covered in the Course
1. Introduction of hardware design methodology, levels of design abstraction, review of logic design and schematics capture.
2. Motivation for design with HDL, VHDL basics: entity, architecture and concurrent statements.
3. Wait statements, variable assignments, signal assignments, VHDL timing model and simulation.
4. VHDL data types, subtypes, operations, process statements and component instantiations.
5. Procedural descriptions, library organization, and packages.
6. Architecture of models, component, and configuration.
7. File input/output, resolved signals, abstract data types.
8. Introduction to programmable devices, differences/commonality between design for ASIC and programmable devices and overview of programmable devices.
9. Discussion on FPGA architecture, design and implementation on FPGAs.
10. Technology mapping, physical design.
11. Design for synthesis, timing back annotation, and verification.

**Laboratory Projects:**
1. Assignments on VHDL structural and behavioral simulation.
2. VHDL based hardware design and FPGA prototyping

**Instructor:**
Dr. Karam S. Chatha,
Office: BY 412
Office hours: MW 3.30-4.30 pm (Exceptions will be announced in class)
Schedule an appointment if these times are not convenient.

Email: Karam.Chatha@asu.edu
Web: http://chatha.faculty.asu.edu/chatha/index.html

**Evaluation policy:**
1. Laboratory assignments – 40 %
2. Mid-term – 30 %
3. Final – 30 %

**Grading policy:**
1. Final score >= 88 % : A
2. 75 % <= Final score < 88 % : B
3. 50 % <= Final score < 75% : C
4. Final score < 50 % : F

**Course page:**
On blackboard.

**EXAM DATES:**
Midterm exam: Class time, March 14th, Wednesday, 2.00-3.15pm.
Final exam: Regular final exam time, (check the ASU website for final exam schedule).